4. The semiconductor device of claim 2, wherein the fuse and the alignment mark are formed within a metal wiring layer of the device.

7. The semiconductor device of claim 1, wherein the etch resistant layer comprises silicon nitride.

8. The semiconductor device of claim 1, wherein the etch resistant layer has a thickness of approximately 10-100 nm.

Remarks

Claims 5-6 have been canceled. Claims 1-4 and 7-8 are currently pending based on the amendment herein, wherein claim 1 has been amended herein.

The specification has been amended herein for clarification purposes. No new matter has been added.

The Examiner rejected claims 1-3 under 35 U.S.C. §102(b) as being anticipated by Takahashi (JP 8-274178).

The Examiner rejected claims 1-4 under 35 U.S.C. §102(b) as being anticipated by Motsiff et al. US Patent No. 5,731,624.

The Examiner rejected claims 1-3 and 5-8 under 35 U.S.C. §102(e) as being anticipated by Narayan et al. US Patent No. 6,127,721.

Applicants respectfully traverse the §102 rejections with the following arguments.

35 U.S.C. §102

Claims 1-3 are rejected under 35 U.S.C. §102(b) as being anticipated by Takahashi (JP 8-274178).

The Examiner alleges that "Takahashi discloses in figs. 1-3 a semiconductor device comprising a substrate 11; at least one fuse 13 formed within the substrate; and an etch resistant layer over the at least one fuse."

As to claim 1 as amended, Applicants respectfully contend that Takahashi does not anticipate claim 1, because Takahashi does not teach each and every feature of claim 1. For example, Takahashi does not teach the features of "a continuous **etch resistant layer** on the surface of the substrate, wherein the etch resistant layer is directly over the at least one fuse; and at least **one insulative layer above** the etch resistant layer, wherein the etch resistant layer has **a slower etch rate** than that of the at least one insulative layer thereabove." (emphasis added). Takahashi does not teach that **an etch resistant layer** is deposited on a surface of a substrate and directly over a fuse embedded within an interior portion of a substrate and that the etch resistant layer has **a slower etch rate** than an insulating layer above the etch resistant layer as described by Applicant's claim 1. In contrast, Takahashi teaches that a fuse is located within a first insulating film formed on a substrate and that a second insulating film is formed on a surface of the first insulating film, as described by Takahashi in the abstract. Furthermore, Takahashi does not even mention an **etch resistant layer** having a **slower etch rate** than an insulating layer above the etch resistant layer. Therefore, Applicants contend that Takahashi does not teach the preceding features of claim 1. Based on the preceding arguments, Applicants respectfully maintain that Takahashi, does not anticipate claim 1, and that claim 1 is in condition for

allowance. Since claims 2-4 and 7-8 depend from claim 1, Applicants contend that claims 2-4 and 7-8 are likewise in condition for allowance.

Claims 1-4 are rejected under 35 U.S.C. §102(b) as being anticipated by Motsiff et al. US Patent No. 5,731,624.

The Examiner alleges that "Motsiff et al. disclose in fig. 1 a semiconductor device comprising a substrate 1; at least one fuse 8 formed within the substrate; and an etch resistant layer 9 over the at least one fuse."

Applicants respectfully contend that Motsiff does not anticipate claim 1, because Motsiff does not teach each and every feature of claim 1. For example, Motsiff does not teach the features of "a continuous **etch resistant layer** on the surface of the substrate, wherein the etch resistant layer is directly over the at least one fuse; and at least **one insulative layer above** the etch resistant layer, wherein the etch resistant layer has **a slower etch rate** than that of the at least one insulative layer thereabove. " (emphasis added). Motsiff does not teach that an **etch resistant layer** is deposited on a surface of a substrate and directly over a fuse embedded within an interior portion of a substrate and that the etch resistant layer has **a slower etch rate** than an insulating layer above the etch resistant layer as described by Applicant's claim 1. In contrast, Motsiff teaches that a fuse is located on a substrate and within an overlayer having the same thickness as the fuse as described by Motsiff in Fig 1C. Furthermore, Takahashi does not even mention an **etch resistant layer** having a **slower etch rate** than **an insulating layer** above the etch resistant layer. If fact, Takahashi does not even mention any second layer (i.e, Applicant's insulating layer) over a fuse. Therefore, Applicants contend that Motsiff does not teach the preceding features of claim 1. Based on the preceding arguments, Applicants respectfully

maintain that Motsiff, does not anticipate claim 1, and that claim 1 is in condition for allowance. Since claims 2-4 and 6-8 depend from claim 1, Applicants contend that claims 2-4 and 7-8 are likewise in condition for allowance.

Claims 1-3 and 5-8 are rejected under 35 U.S.C. §102(e) as being anticipated by Narayan et al. US Patent No. 6,127,721.

The Examiner alleges that "Narayan et al. disclose (see figs. 1 and 2 and col. 3, lines 41-50) a semiconductor device comprising a substrate 101; at least one fuse 120 formed within the substrate; and an etch resistant layer 130 or silicon nitride (as in claim 7) having a thickness which falls within a range recited in the claim (as in claim 8) over the at least one fuse."

Applicants respectfully contend that Narayan et al. does not anticipate claim 1, because Narayan et al. does not teach each and every feature of claim 1. For example, Narayan does not teach the feature of "at least one fuse **embedded** within an interior portion of the substrate; a **continuous** etch resistant layer on the surface of the substrate, wherein the etch resistant layer is directly **over** the at least one fuse; and at least one insulative layer above the etch resistant layer, wherein the etch resistant layer has a slower etch rate than that of the at least one insulative layer thereabove." (emphasis added). Narayan does not teach that a fuse is **embedded** within an interior portion of a substrate and that a **continuous** etch resistant layer is deposited on a surface of the substrate and directly **over** the fuse as described by Applicant's claim 1. In contrast, Narayan teaches a **sectioned** (i.e., not continuous) etch stop layer used to define a via opening as described by Narayan in the abstract and Figs 1 and 2. Additionally, Narayan teaches that a "device feature" (e.g, a fuse) is located within the via opening defined by the sectioned etch stop layer, therefore the etch stop layer may not be **over** the fuse as described by Applicant's claim 1.

Furthermore, Narayan teaches that the device feature within the via opening is **smaller** than the via opening and therefore Applicant's contend that the device feature is not **embedded** within the substrate as described by Applicant's claim 1. Therefore, Applicants contend that Narayan does not teach the preceding features of claim 1. Based on the preceding arguments, Applicants respectfully maintain that Narayan, does not anticipate claim 1, and that claim 1 is in condition for allowance. Since claims 2-4 and 7-8 depend from claim 1, Applicants contend that claims 2-4 and 7-8 are likewise in condition for allowance.

Conclusion

Based on the preceding amendments and arguments, Applicant respectfully believes that claims 1-4, 7-8 and the entire application, are in condition for allowance and therefore request favorable action. However, should the Examiner believe anything further is necessary in order to place the application in better condition for allowance, or if the Examiner believes that a telephone interview would be advantageous to resolve the issues presented, the Examiner is invited to contact the Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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Appendix A. Identification of Amended Material

Claim 1 is amended as follows:

1. (Amended) A semiconductor device comprising:

a substrate;

at least one fuse embedded [formed] within an interior portion of the substrate; [and]

[an] a continuous etch resistant layer on a surface of the substrate, wherein the etch resistant layer is directly over the at least one fuse; and

at least one insulative layer above the etch resistant layer, wherein the etch resistant layer has a slower etch rate than that of the at least one insulative layer thereabove.